



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER OF PATENTS AND TRADEMARKS  
Washington, D.C. 20231  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/539,839	03/31/2000	Ariel Berkovits	2207/6856	9593

7590

02/19/2003

Kenyon & Kenyon  
333 W San Carlos Street  
Suite 600  
San Jose, CA 95110-2711

EXAMINER

PEUGH, BRIAN R

ART UNIT

PAPER NUMBER

2187

DATE MAILED: 02/19/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/539,839

Applicant(s)

BERKOVITS, ARIEL

Examiner

Brian R. Peugh

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 28 January 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Response to Amendment***

This Office Action is in response to applicant's communication filed January 28, 2003, in response to PTO Office Action dated May 8, 2002. The applicant's remarks and amendment to the specification and/or claims were considered with the results that follow.

Claims 1-30 have been presented for examination in this application.

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn.

### ***Claim Rejections - 35 USC § 102***

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-5, 9-13, 17-21, and 25-30 are rejected under 35 U.S.C. 102(b) as being anticipated by Csoppenszky (US# 5,802,568).

Regarding claims 1, 9, 17, 25, 26, and 30, Csoppenszky teaches pseudo-LRU caching system including an invalidation scheme in associative caches. Figures 2 and 3 portray a system for lowering the importance level of cache lines. When an operation for replacing a cache line begins, the memory is searched first for invalid items. Should

Art Unit: 2187

all of the memory items be both valid and have their used bits set, all used bits are cleared except the bit indicated by signal ADDR from multiplexor (125) (col. 4, line 22 – col. 5, line 32). Thus, the importance level of all lines save that of the line indicated by the signal ADDR have been decreased and are available for replacement. Regarding claim 17 specifically, one of ordinary skill in the art would appreciate that for any type of replacement system to occur, here a pseudo-LRU with a valid-used bit clearing replacement scheme, the conditions and operational instructions necessary for the replacement system to work must be stored within a data storage system within the computing system. Since the replacement system of Csoppenszky includes the above-mentioned scheme, the replacement system must inherently store the means for which to do so in any number of locations, such as on the processor itself or within an external data storage device. Specifically regarding claim 25, although not explicitly stated, for cache operations to occur on cache lines with corresponding (valid) bits, some form of cache control logic must be present and therefore would be inherent to the teaching of Csoppenszky.

Regarding claims 2, 10, 18, 27, and 30, the importance level of the cleared cache lines have been decreased in accordance with the procedure for finding a suitable replacement line when an instruction requires a memory line for access when all lines have their used and valid bits selected high.

Regarding claims 3, 11, 19, and 28, cache lines with cleared used bits are replaced before the line indicated by signal ADDR according to the LRU scheme, since the line indicated by the signal ADDR is indicated as the most recently used entry.

Art Unit: 2187

Also, since all lines having had their used bits cleared, and the used and validity bits do not indicate the order in which entries were used or which entry was least recently used, an item selected for replacement (with used bit cleared) could have been selected before another item (with used bit cleared) according to the LRU policy (col. 4, lines 50-54).

Regarding claims 4, 12, and 20, the replacement policy as noted above is an LRU policy. As recited above, the clearing of the used bit makes it possible that the least recently used item may not be selected before another item that was more recently used.

Regarding claims 5, 13, 21, and 29, since all lines having had their used bits cleared, and the used and validity bits do not indicate the order in which entries were used or which entry was least recently used, an item selected for replacement (with used bit cleared) could have been selected before another item (with used bit cleared) according to the LRU policy (col. 4, lines 50-54). Thus, the allocation methodology according to the LRU policy has been altered.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Art Unit: 2187

Claims 6, 7, 14, 15, 22, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Csoppenszky (US# 5,802,568) and Funk et al. (US# 6,314,561).

The difference between the claimed subject matter and that of Csoppenszky, disclosed supra, is that the claims recite that the replacement instruction is generated by a compiler or is part of an application kernel. Regarding claims 7, 15, and 23, Funk et al. teaches a data cache management mechanism that is created by an optimizing compiler. The compiler places non-blocking preload instructions into the instruction stream of the computer system so as to minimize both the frequency and detrimental effect of cache misses (column 3, lines 17-22). Thus, the compiler hopes to minimize cache misses by loading data from the main memory into the cache. This directly relates to the cache loading and replacement scheme of Csoppenszky. The creation of the data cache management mechanism relates to the claimed material of claims 6, 14, and 22, in that a kernel is a core processing mechanism used within a computer system. The optimization compiler of Csoppenszky sends commands for optimizing the caching system as well as controlling the data cache management mechanism, such that parts of the mechanism are present in all mechanism that were compiled by the optimization compiler (column 6, line 66 – column 7, line 11). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Csoppenszky and Funk et al. before him at the time the invention was made to modify the caching system of Csoppenszky to include the optimization compiler/data cache management mechanism of Funk et al., because then instruction could be pre-loaded into the

Art Unit: 2187

instruction stream in order to curb the frequency of cache misses, as taught by Funk et al.

Claims 8, 16, and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Csoppenszky (US# 5,802,568) and Worley, Jr. et al.

The difference between the claimed subject matter and that of Csoppenszky, disclosed supra, is that the claims recite that an instruction for designating replacement is an extension of a memory access instruction. Worley, Jr. et al. teaches a caching system with a corresponding flush data cache instruction. In order to flush, the item must first be selected for removal, hence the extension. The cache line is written back to main memory if the cache line's dirty bit is set (column 4, lines 36-40). Therefore it would have been obvious to one of ordinary skill in the art having the teachings of Csoppenszky and Worley, Jr. et al. before him at the time the invention was made to modify the caching and clearing scheme of Csoppenszky to include the flush data cache instruction of Worley, Jr. et al., because then a system for writing back altered data to the main memory would be in place that would negate the loss of potentially important information, as taught by Worley, Jr. et al.

### ***Response to Arguments***

Applicant's arguments with respect to claims 1-30 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.


Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brian R. Peugh whose telephone number is 703-306-5843. The examiner can normally be reached on Monday-Thursday from 7:00am to 4:30pm. The examiner can also be reached on alternate Friday's from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Do Yoo, can be reached on (703) 308-4908. The fax phone number for the organization where this application or proceeding is assigned is 703-746-7239.

Art Unit: 2187

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-9600.

  
DY/BRP  
February 10, 2003

  
MATTHEW KIM  
SUPERVISORY PATENT EXAMINER  
TECHNOLOGY CENTER 2100